REMARKS

This amendment responds to the office action mailed January 22, 2008. In the final office action the Examiner:

- rejected claims 21-24 and 26-34 under 35 U.S.C. 102(e) as being anticipated by Darwish (US 6,764,906)
- allowed claims 15-20; and
- objected to claim 25 as being dependent upon a rejected base claim.

After entry of this amendment, the pending claims are: claims 15-34.

Phone Interview

On April 21, 2008, the applicant's attorneys, Gary S. Williams (Reg. No. 31,066) and Yalei Sun (Reg. No. 57,765), had a phone interview with the Examiner. During the interview, the applicant's attorneys explained that Darwish teaches the structure of a power MOSFET (Fig. 1 of Darwish) and a fabrication method (Fig. 18 of Darwish). But Darwish does not teach the claim element of the first gate region and the second gate region forming a dual gate structure, which is present in all the pending claims. The Examiner agreed that Darwish lacks the teaching of the dual gate structure.

Claim Rejections - 35 U.S.C. 102(e)

The Examiner argued that Darwish anticipates pending claims 21-24 and 26-34. The applicant respectfully traverses.

Darwish relates to a trench-gated power MOSFET and a process for manufacturing a power MOSFET. *See* col. 1, lines 11-14. Figure 1 of Darwish (reproduced below) and related text explains the structure of a typical trench-gated power MOSFET 10:

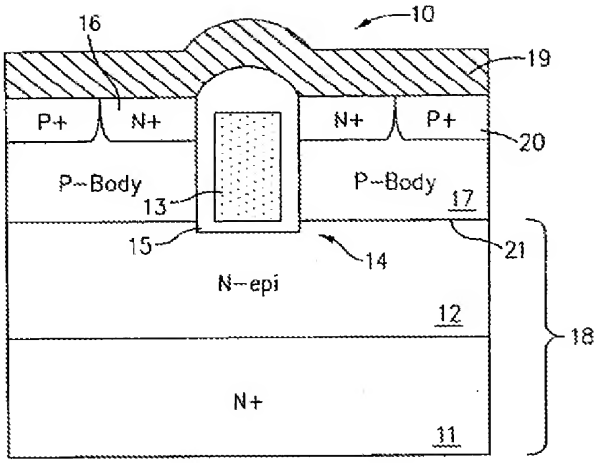

FIG. 1
(PRIOR ART)

In particular, the gate 13 is formed in a trench 14 which extends downward from the top surface of the N-epi layer 12. The gate 13 is made of polysilicon and is electrically isolated from the N-epi layer 12 by an oxide layer 15. The N-epi layer 12 is part of the drain-drift region 18 of the trench-gated power MOSFET 10. *See* col. 1, lines 17-34.

Figure 18 of Darwish (reproduced below) and related text does not teach a **dual gate structure** as recited in all the pending claims. Regions 124A, 124B, and 124C, which the Examiner referred to as "first gate region," "buffer region," and "second gate region," respectively, are actually **a stack of implanted N regions** used for forming the drain-drift region. *See* col. 8, lines 1-10. These N regions are an extension of the N+ drain region 102 (see Figure 18 below). By definition, none of the implanted N regions are gate regions and they cannot form a dual gate structure because the gate of the trench-gated power MOSFET is formed in the trench above the implanted N regions and electrically isolated from the substrate.

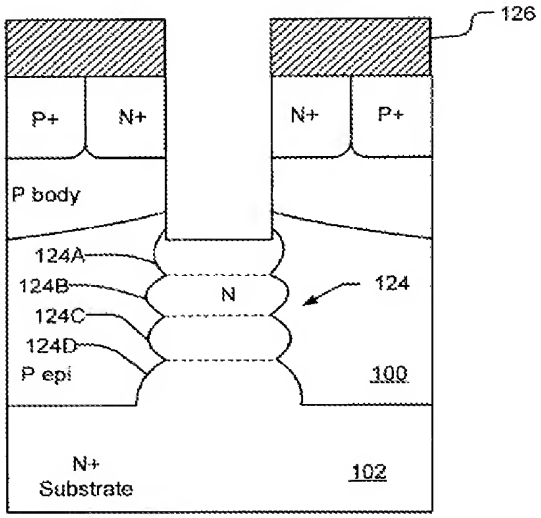

Fig. 18

Because Darwish does not teach or suggest the formation of a dual gate structure as recited in the pending claims, claims 21-34 are not anticipated by Darwish.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 21, 2008

/ Gary S. Williams / 31,066

Gary S. Williams (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square
3000 El Camino Real, Suite 700
Palo Alto, CA 94306
(650) 843-4000